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(to be used for all correspondence after initial filing)

Application Number	09/920,891
Filing Date	August 2, 2001
First Named Inventor	Michael Kwan
Art Unit	1763
Examiner Name	Kackar, Ram N.
Attorney Docket Number	A4231/T34410

Total Number of Pages in This Submission

ENCLOSURES ***(Check all that apply)***

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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- ☐ After Allowance Communication to Group
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- ☐ Proprietary Information
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- ☒ Other Enclosure(s) *(please identify below)*:

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Firm or Individual	Townsend and Townsend and Crew LLP Patrick M. Boucher Reg. No. 44,037
Signature	Patrick Boucher
Date	September 15, 2003

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FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT | ($) 320

Complete If Known	
Application Number	09/920,891
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First Named Inventor	Michael Kwan
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Art Unit	1763
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METHOD OF PAYMENT *(check all that apply)*

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☒ Deposit Account:

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims	Fees from below	Fee Paid
Total Claims		-** =		X =	
Independent Claims		-** =		X =	
Multiple Dependent				X =	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive – unavoidable	
1453	1,300	2453	650	Petition to revive – unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Petitions related to provisional applications	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR § 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

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*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($)320

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Patrick M. Boucher	*Registration No. (Attorney/Agent)*	44,037	*Telephone*	303-571-4000
Signature	Patrick Boucher			*Date*	September 15, 2003

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By Nina L. McNeill
Nina L. McNeill

PATENT
Attorney Docket No.: A4231/T34410
AMAT No.:
A4231/USA/D01/DSM/HDP/CVD/JW
TTC No.: 016301-034410US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:

Michael Kwan et al.

Application No.: 09/920,891

Filed: August 2, 2001

For: GAS CHEMISTRY CYCLING TO ACHIEVE HIGH ASPECT RATIO GAPFILL WITH HDP-CVD

Examiner: Kackar, Ram N.

Art Unit: 1763

APPELLANT BRIEF UNDER 37 CFR §1.192

Mail Stop Appeal Brief - Patents
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Alexandria, VA 22313-1450

Sir:

Appellant offers this Brief further to the Notice of Appeal mailed on July 14, 2003. This Brief is submitted in triplicate as required by 37 CFR §1.192(a).

1. Real Party in Interest

The real party in interest is Applied Materials, Inc.

2. Related Appeals and Interferences

No other appeals or interferences are known that will directly affect, are directly affected by, or have a bearing on the Board decision in this appeal.

3. Status of Claims

Claims 17 – 22 are pending in the application and stand finally rejected by the Examiner. The application is a divisional of U.S. Pat. No. 6,335,288 ("the parent patent"); Claims 1 – 16 were canceled by preliminary amendment since they correspond to claims issued in the parent patent. No amendments have been made to the currently pending claims during the prosecution of the application.

4. Status of Amendments

No amendments have been filed subsequent to the final rejection mailed April 22, 2003.

5. Summary of the Invention

The claimed invention relates generally to filling high-aspect-ratio gaps during the manufacture of integrated circuits on a substrate (Application, p. 1, ll. 6 – 7). As semiconductor device geometries have decreased in size over the years, the aspect ratio of gaps that require filling, i.e. the ratio of the height of such gaps to their width, have increased dramatically at the same time that the width of such gaps has decreased. This development has presented the semiconductor industry with a particular challenge to develop techniques for filling such gaps without the formation of interior voids, which can adversely affect the performance of the completed devices (*id.*, p. 2, ll. 4 – 6).

The claims are directed to a computer-readable storage medium and a substrate processing system that include a computer-readable program having instructions to implement a process capable of filling such aggressive gaps. The process cycles a gas chemistry to interleave deposition and etching steps in what is sometimes referred to in the art as a "dep/etch/dep" process (*see id.*, p. 16, ll. 5 – 6). The etch step that intervenes between the deposition steps acts to partially reopen the gap after the initial deposition so that material may be deposited in the gap by the subsequent deposition without forming a void. The dep/etch/dep process is integrated with a high-density-plasma chemical-vapor-deposition ("HDP-CVD") process that inherently includes simultaneous deposition and sputtering characteristics (*id.*, p. 16, ll. 6 – 8). It is because of this inherent simultaneity of deposition and sputtering characteristics that the integration of a dep/etch/dep process with an HDP-CVD process was traditionally dismissed in the art as inutile (*see id.*, p. 3. ll. 1 – 8).

In addition to integrating these disparate processes, the claims require a separate cooling step in which the temperature of the substrate is lowered after the initial deposition and before the etching (*id.*, p. 20, ll. 11 – 13). By achieving a temperature reduction of the substrate even before the etching step is begun, a more controlled etch may be achieved (*id.*, p. 20, ll. 13 – 14), thereby further improving the gapfill characteristics of the process.

6. Issue

Whether under 35 U.S.C. §103(a) Claims 17 – 22 are unpatentable over U.S. Pat. No. 5,990,000 issued to Hong *et al.* (hereinafter "Hong") in view of U.S. Pat. No. 6,030,881 issued to Papasouliotis *et al.* (hereinafter "Papasouliotis").

7. Grouping of the Claims

For purposes of this appeal, Claims 17 – 22 are considered as a single group. Appellant reserves the right outside the context of this appeal to argue independent patentability of any of the grouped claims.

8. Argument

All the pending claims stand rejected under 35 U.S.C. §103(a) as unpatentable over Hong in view of Papasouliotis. To support a rejection under 35 U.S.C. §103, the Examiner is charged with factually supporting a *prima facie* case of obviousness. Manual of Patent Examining Procedure, Eighth Edition, First Revision, February, 2003 (hereinafter "MPEP") 2142. Such a *prima facie* case requires that all limitations of the claims be taught or suggested by the cited references, that there be some suggestion or motivation to combine or modify the reference teachings as the Examiner proposes, and that there be a reasonable expectation of success. MPEP 2143. The rejections are deficient in all these respects.

Hong is the principal reference relied on and discloses a plasma-enhanced chemical-vapor-deposition ("PECVD") dep/etch/dep process in which the etching is a multiple etch that includes both chemical and physical phases (Hong, Col. 2, ll. 24 – 36). This is similar to the prior art addressed by Appellants in the their application (Application, p. 2, ll. 16 – 26). The Examiner relies on Hong for its disclosure of a computer-readable storage medium for controlling the PECVD dep/etch/dep process (*see, e.g.*, Final Office Action mailed April 22, 2003 (the "Office Action"), p. 2). This teaching is combined with Papasouliotis, which is cited primarily for its disclosure of using a mixture of deposition and inert gases during the deposition portion of the process, and for using a technique during the deposition portion that has both deposition and sputter components (*id.*, p. 2).

a. Neither Hong nor Papasouliotis Teach or Suggest a Separate Cooling Step

Throughout the prosecution of the application, Appellants have emphasized repeatedly that the cited prior art fails to disclose a separate cooling step and have challenged the Examiner to provide a reference drawn from the dep/etch/dep art that discloses such a step. Without such a disclosure, the requirements for a *prima facie* case have simply not been met. In response, the Examiner has cited language in Papasouliotis and has cited a number of patents, none of which makes the required disclosure.

For example, the following language in Papasouliotis has been cited as teaching that "a temperature change will be needed" (Office Action, p. 4):

> [T]ransitions from a deposition to an etching step are effected by varying the composition of the mixture, the power supplied to the wafer, the chamber pressure, and/or the temperature of the wafer.
> (Papasouliotis, Col. 8, ll. 42 – 45).

This language merely states that the deposition and etching steps are characterized by differences in various process conditions, one of which might, but need not, include temperature ("and/or"). The plain language explicitly contemplates that no change in temperature might be made if other process conditions are changed to effect an etching step. Accordingly, the statement in the Office Action that Papasouliotis expresses a "need" to change the temperature before the etching is simply incorrect.

In other instances, the Examiner has cited art that admittedly uses the word "cooling" in referring to an etching process, but in a manner that plainly indicates that a temperature is being maintained to offset an external source of heat. These references do not disclose "cooling" in the sense of reducing the temperature as is intended by the claim language (*see* Application, p. 20, ll. 11 – 14). For instance, the following language was cited from U.S. Pat. No. 5,316,278 (hereinafter "Sherstinsky"):

> In the plasma etching of semiconductor wafers, it is conventional to cool the wafer (*or more properly to maintain it at a preselected temperature*) during the etch process by flowing a gas, e.g., helium or argon, through an opening in the underlying cathode support pedestal to the space between the top surface of the pedestal and the undersurface (backside) of the wafer. The presence of such a gas in this space serves t[o] enhance the thermal coupling of the wafer to the underlying pedestal which serves to cool the wafer,

> i.e. *to maintain it at a preselected temperature* despite heat generated by the plasma etching being carried out on the top surface of the wafer.
> (Sherstinsky, Col. 1, ll. 15 – 26, emphasis added).

This language makes it unmistakably clear that Sherstinsky is referring to "cooling" merely to counteract the plasma heat and thereby maintain a constant temperature of the wafer during etching. Similarly, the following language was cited from U.S. Pat. No. 6,310,755 (hereinafter "Kholodenko"):

> In certain processes, it is also desirable to rapidly cool the substrate *in order to maintain the substrate in a narrow range of temperatures*, especially for etching interconnect lines that have very small dimensions and are positioned close together.
> (Kholodenko, Col. 1, ll. 56 – 60, emphasis added).

The emphasized language makes it clear that Kholodenko is referring to "cooling" in the same sense as Sherstinsky — an approximately constant temperature is being maintained during the etching step. The Examiner's assertion that "Kholodenko goes even further and clearly teaches the desirability of cooling rapidly *before etch*" (Office Action , p. 5, emphasis added) is unsupported by any citation to Kholodenko. Appellants believe that there is no disclosure of cooling before etching in Kholodenko and that its disclosure is limited to teaching maintaining a temperature during an etch.[1]

The Examiner also fails to give due weight to the fact that the claim language separates the cooling step from the deposition and etching steps by using

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[1] Earlier in the prosecution, the Examiner also cited U.S. Pat. No. 6,015,760 (hereinafter "Becker") to show that chemical etching characteristics depend on temperature (Office Action mailed June 24, 2002, pp. 3 – 4). Notably, Becker is actually an example in which the desired etch characteristics are achieved by heating the substrate (Becker, Col. 2, ll. 54 – 67). This illustrates that the particular temperature characteristics of an etching process depend intimately on the desired application and other process conditions, underscoring the need for any a *prima facie* case under §103 to be supported by a teaching of a cooling step drawn from the dep/etch/dep.

Later in the prosecution, the Examiner cited U.S. Pat. No. 6,268,274 (hereinafter "Wang"), but withdrew the rejections based on Wang after Appellants pointed out that the cooling was described there for a sequence of steps exactly opposite to that claimed (Response filed April 2, 2003, pp. 3 – 4).

These facts are especially notable since the Examiner concedes that "Papasouliotis [does] not explicitly disclose that the changing of temperature would be a cooling step" (Office Action mailed January 2, 2003, p. 4) and is obligated to "consider[] the degree to which one reference might accurately discredit another" when "the teachings of two or more prior art references conflict." MPEP 2143.01.

"thereafter" language to delineate it from those steps. "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970). For example, the language cited above from Papasouliotis speaks only to a "transition," which suggests a continuous change from a deposition phase to an etching phase as the process conditions are altered. The Examiner's position that "every transition is a separate instruction and a separate step" (Office Action, p. 4) is untenable. Clearly, transitions can and frequently do take place continuously through changes in processing conditions as suggested by Papasouliotis. At every point during such a transition, the process conditions define a certain deposition/sputter ratio (*see* Application, p. 16, ll. 12 – 20 and Papasouliotis, Col. 3, ll. 22 – 23) so that the process is either in a deposition or an etching phase. This is not the case with the invention as claimed, in which a deposition step is concluded so that "thereafter" the substrate may be cooled and "thereafter" a separate etching step may be begun.

b. There is no Motivation to Combine Hong with Papasouliotis in the Manner Suggested and No Reasonable Expectation of Success

Fundamental to the requirement that there be a motivation to combine references is that the prior art suggest the desirability of the claimed invention, coupled with a reasonable expectation of success. MPEP 2143.01. While often treated as two separate prongs of the *prima facie* case, it is convenient here to treat these requirements collectively. "In determining the propriety of the Patent Office case for obviousness in the first instance, it is necessary to ascertain whether or not the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the reference before him to make the proposed substitution, combination, or other modification." MPEP 2143.01, *citing In re Linter*, 173 USPQ 560, 562 (CCPA 1972). In this instance, Papasouliotis specifically cautions *against* combining its teachings with those describing PECVD dep/etch/dep processes (*see generally* Papasouliotis, Col. 2, ll. 11 – 57). Papasouliotis draws a number of distinctions between PECVD and HDP-CVD processes,

cautioning that "[t]he differences in the physics and chemistry of PECVD and HDP processes result in significant differences in the growth of the deposited film" (Papasouliotis, Col. 2, ll. 36 – 38).

These admonitory statements against the equivalence of HDP-CVD and PECVD steps in a dep/etch/dep process cannot simply be disregarded. "A prior art reference must be considered in its entirety, i.e. as a whole, including portions that would lead away from the claimed invention." MPEP 2141.02, *citing W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984) (emphasis in original). In responding to this argument when it was presented during prosecution of the application, the Examiner stated the following:

> Papasouliotis does not teach away either from Hong or the application and suggests improvement to the simple dep/etch/dep process of Hong in the same way as done by the applicant. Both recognized the dep/etch/dep process to be a prior art and having limitations in filling gap [*sic*] of higher aspect ratios.
> (Advisory Action mailed September 6, 2002)

It is clear from these comments that the Examiner is influenced by perceived similarities of the solution ultimately proposed by Papasouliotis with aspects of Hong, namely that they both use dep/etch/dep processes. This amounts to the use of impermissible hindsight reasoning to supply the motivation and is contrary to the express teachings of the reference relied on. Since Papasouliotis specifically suggests that there is *no* expectation of success in performing a combination with a PECVD dep/etch/dep process, no *prima facie* case has been established.

9. Conclusion

Appellant believes that the above discussion is fully responsive to all grounds of rejection set forth in the application. Please deduct the requisite fee of $320.00 pursuant to 37 C.F.R. §1.17(c) from Deposit Account 20-1430 and any additional fees that may be due in association with the filing of this Brief.

Respectfully submitted,

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APPENDIX

The claims pending in the application are as follows:

17. (Unchanged) A computer-readable storage medium having a computer-readable program embodied therein for directing operation of a substrate processing system including a process chamber; a plasma generation system; a substrate holder; and a gas delivery system configured to introduce gases into the process chamber, the computer-readable program including instructions for operating the substrate processing system to deposit a dielectric film on a substrate disposed in the process chamber in accordance with the following:

(a) providing a first gaseous mixture to the process chamber, the first gaseous mixture comprising a first deposition gas and a first inert gas source;

(b) generating a first high-density plasma from the first gaseous mixture to deposit a first portion of the film on the substrate with a first deposition/sputter ratio within the range of 5 – 12, wherein the first deposition/sputter ratio is defined as a ratio of a sum of a first net deposition rate and a first blanket sputtering rate to the first blanket sputtering rate;

(c) thereafter, cooling the substrate;

(d) thereafter, flowing an etchant gas into the process chamber;

(e) thereafter, providing a second gaseous mixture to the process chamber, the second gaseous mixture comprising a second deposition gas and a second inert gas source; and

(f) generating a second high-density plasma from the second gaseous mixture to deposit a second portion of the film on the substrate.

18. (Unchanged) The computer readable storage medium according to claim 17 wherein the second high-density plasma is generated to deposit the second

portion of the film with a second deposition/sputter ratio within the range of 5 – 20, wherein the second deposition/sputter ratio is defined as a ratio of a sum of a second net deposition rate and a second blanket sputtering rate to the second blanket sputtering rate.

19. (Unchanged) The computer-readable storage medium according to claim 17 wherein the dielectric film is to be deposited over a plurality of stepped surfaces formed on the substrate having gaps formed between adjacent ones of the stepped surfaces and wherein the first portion of the film partially fills the gaps.

20. (Unchanged) A substrate processing system comprising:

(a) a housing defining a process chamber;

(b) a high-density plasma generating system operatively coupled to the process chamber;

(c) a substrate holder configured to hold a substrate during substrate processing;

(d) a gas-delivery system configured to introduce gases into the process chamber;

(e) a pressure-control system for maintaining a selected pressure within the process chamber;

(f) a controller for controlling the high-density plasma generating system, the gas-delivery system, and the pressure-control system; and

(g) a memory coupled to the controller, the memory comprising a computer-readable medium having a computer-readable program embodied therein for directing operation of the substrate processing system, the computer-readable program including

(i) instructions to control the gas-delivery system to provide a first gaseous mixture to the process chamber, the first gaseous mixture comprising a first deposition gas and a first inert gas source;

(ii) instructions to control the high-density plasma generating system to generate a first high-density plasma from the first gaseous mixture to deposit a first portion of the film on the substrate with a first deposition/sputter ratio within the range of 5 – 20, wherein the first deposition/sputter ratio is defined as a ratio of a sum of a first net deposition rate and a first blanket sputtering rate to the first blanket sputtering rate;

(iii) instructions to control the gas-delivery system thereafter to flow a heat-transfer gas to cool the substrate;

(iv) instructions to control the gas-delivery system thereafter to flow an etchant gas into the process chamber;

(v) instructions to control the gas-delivery system thereafter to provide a second gaseous mixture to the process chamber, the second gaseous mixture comprising a second deposition gas and a second inert gas source; and

(vi) instructions to control the high-density plasma generating system to generate a second high-density plasma from the second gaseous mixture to deposit a second portion of the film on the substrate.

21. (Unchanged) The substrate processing system according to claim 20 wherein the instruction to generate a second high-density plasma comprise instructions to deposit the second portion of the film with a second deposition/sputter ratio within the range of 5 – 20, wherein the second deposition/sputter ratio is defined as a ratio of a sum of a second net deposition rate and a second blanket sputtering rate to the second blanket sputtering rate.

22. (Unchanged) The substrate processing system according to claim 20 wherein the dielectric film is to be deposited over a plurality of stepped surfaces formed on the substrate having gaps formed between adjacent ones of the stepped surfaces and wherein the first portion of the film partially fills the gaps.